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Description

HIGH-DENSITY FINFET INTEGRATION SCHEME

BACKGROUND OF INVENTION

[0001] Field of the Invention

[0002] The present invention generally relates to transistors and more particularly to the fin type transistors known as FinFETs and to an improved manufacturing process and FinFET structure.

[0003] Description of the Related Art

[0004] As the need to decrease the size of transistors continues, new and smaller types of transistors are created. One recent advance in transistor technology is the introduction of fin type field effect transistors that are known as FinFETs. U.S. patent 6,413,802 to Hu et al. (hereinafter "Hu"), which is incorporated herein by reference, discloses a FinFET structure that includes a center fin that has a channel along its center and source and drains at the ends of the fin structure. A gate conductor covers the channel portion.

[0005] While FinFETs structures reduce the size of transistor-based devices, it is still important to continue to reduce the size of FinFETs transistors. The invention described below provides a method and structure which

decreases the distance between adjacent FinFETs, thereby reducing the overall size of the transistor-based structure.

SUMMARY OF INVENTION

[0006] The invention provides a method of manufacturing a fin-type field effect transistor (FinFET) that begins by patterning a rectangular sacrificial mandrel on a substrate. Next, the invention forms mask sidewalls along the vertical surfaces of the mandrel. Subsequently, the mandrel is removed and the portions of the semiconductor layer not protected by the mask sidewalls are etched to leave a freestanding rectangular loop of semiconductor material having two longer fins and two shorter sections. The process continues by patterning a rectangular gate conductor over central sections of the two longer fins, wherein the gate conductor intersects to the two longer fins. Next, the invention dopes portions of the semiconductor material not covered by the gate conductor to form source and drain regions in portions of the fins that extend beyond the gate. Following this, the invention forms insulating sidewalls along the gate conductor.

[0007] Then, the invention covers the gate conductor and the semiconductor material with a conductive contact material and forms a contact mask over a portion of the conductive contact material that is above source and drain regions of a first fin of the two longer fins. The invention follows this by selectively etching regions of the conductive contact material and the semiconductor material not protected by the contact mask. This leaves the conductive contact material on source and drain

regions of the first fin and removes source and drain regions of a second fin of the two longer fins.

[0008] This process forms a unique FinFET that has a first fin with a central channel region and source and drain regions adjacent the channel region, a gate structure intersecting the first fin and covering the channel region, and a second fin having only a channel region. The second fin is parallel to the first fin and covered by the gate.

[0009] In this unique structure, the second fin has a length equal to the width of the gate structure and the first fin is longer than the second fin. The source and drain regions of the first fin extend beyond the gate structure; however, the second fin does not extend beyond the gate. The source and drain contacts only cover the source and drain regions of the first fin and no contacts are positioned adjacent the second fin.

BRIEF DESCRIPTION OF DRAWINGS

[0010] The foregoing and other objects, aspects and advantages will be better understood from the following detailed description of a preferred embodiment(s) of the invention with reference to the drawings, in which:

[0011] Figure 1A is a schematic top-view diagram of a partially completed FinFET structure according to the invention;

[0012] Figure 1B is a cross-sectional view along line A-A' in Figure 1A;

[0013] Figure 1C is a cross-sectional view along line B-B' in Figure 1A;

[0014] Figure 2A is a schematic top-view diagram of a partially completed FinFET structure according to the invention;

[0015] Figure 2B is a cross-sectional view along line A-A' in Figure 2A;

[0016] Figure 2C is a cross-sectional view along line B-B' in Figure 2A;

[0017] Figure 3A is a schematic top-view diagram of a partially completed FinFET structure according to the invention;

[0018] Figure 3B is a cross-sectional view along line A-A' in Figure 3A;

[0019] Figure 3C is a cross-sectional view along line B-B' in Figure 3A;

[0020] Figure 4A is a schematic top-view diagram of a partially completed FinFET structure according to the invention;

[0021] Figure 4B is a cross-sectional view along line A-A' in Figure 4A;

[0022] Figure 4C is a cross-sectional view along line B-B' in Figure 4A;

[0023] Figure 4D is a cross-sectional view along line C-C' in Figure 4A;

[0024] Figures 5A is a schematic perspective view illustrating the inventive fins intersecting the gate;

[0025] Figures 5B is a schematic top-view diagram of the structure shown in Figure 5A;

[0026] Figure 6A is a schematic top-view diagram illustrating the spacing that is required when a conventional trim mask is utilized;

[0027] Figure 6B is a schematic top-view diagram illustrating the spacing that

can be achieved with the invention when the use of a trim mask is avoided; and

[0028] Figure 7 is a flow diagram illustrating a preferred method of the invention.

DETAILED DESCRIPTION

[0029] Since the silicon fins in FinFETs are significantly thinner than the gate length, non-conventional means of defining the fin thickness are useful. The invention uses a Sidewall Image Transfer (SIT) process for the purpose of forming the fins. Since all shapes left on the wafer from SIT processing are in the form of loops, a trim mask (TR) is necessary to remove unwanted fins shapes that are formed during sidewall image transfer processing. Trim masks break the loops into lines with ends. The trim mask requires critical image tolerance and placement. Therefore, the trim mask is costly and can decrease yield. Furthermore, the trim mask adds requirements to other overlays since the trimmed fins are second-order alignments to later masks. The invention described below eliminates the need to use such a trim mask.

[0030] As mentioned above, the invention forms fins for a FinFET device using sidewall image transfer processing, yet the invention eliminates the need for a separate trim mask. Instead, the invention trims the unwanted portions of the loop structure formed during the sidewall image transfer processing using the same mask that defines the source and drain contacts. The inventive methodology begins by patterning a rectangular sacrificial mandrel 10 on a hard-mask layer 16 that overlies

a layer of semiconductor material 11, as shown in Figure 1A. Next, the invention forms sidewall spacers 12 along the vertical surfaces of the mandrel 10. The sidewall spacers 12 are formed by depositing a masking material and then performing a selective anisotropic etching process that removes material from horizontal surfaces at substantially higher rates than it removes material from vertical surfaces. This process leaves the deposited mask material 12 only along the sides of the mandrel 10, as shown in Figures 1A. Subsequently, the mandrel 10 is removed, the hard-mask material 16 is etched using the spacers 12 as masks, and the spacers 12 are removed to leave a freestanding rectangular loop of mask material 16 having two longer sections 15 and two shorter sections 14.

[0031] An etching process is used to remove portions of the underlying semiconductor material 11 not protected by the mask 16. This leaves a freestanding rectangular loop of semiconductor material 11 covered by the mask material 16 as most clearly shown in Figures 1B and 1C. Figure 1A is a top-view of the structure, Figure 1B is a cross-sectional view along line A-A' in Figure 1A, and Figure 1C is a cross-sectional view along line B-B' in Figure 1A. The longer fins 21 of semiconductor material 11 are perpendicular to the shorter sections 22 of the semiconductor material 11.

[0032] The process continues by patterning a rectangular gate conductor 20 over central sections of the two longer fins 21, wherein the gate conductor 20 intersects the two longer fins 21, as shown in Figures 2A-

2C . Next, the invention dopes portions of the semiconductor loop 11 not covered by the gate conductor 20 to form conductive source and drain regions in portions of the longer fins 21 that extend beyond the gate 20. Following this, the invention forms insulating sidewalls 31 along the gate conductor 20, as shown in Figure 3C. The spacers 31 and gate 20 are sometimes referred to herein as a gate structure.

[0033] Then, the invention covers the gate conductor 20 and the semiconductor material 11 with a conductive contact material 30 (such as polysilicon) as shown in Figures 3A-3C. As most clearly shown in Figures 3B and 3C, the conductive material 30 completely covers the fin structures 11, yet has a height less than that of the gate 20 and spacers 31. The conductive material 30 should not cover the gate 20, otherwise the gate 20 may be shorted to the source and drain contacts. The conductive material 30 can either be selectively deposited so as not to exceed the height of the gate 20 or can be subsequently recessed below the height of the gate 20 using well known etching or overpolishing processes.

[0034] Next, as shown Figure 4A, the invention forms a contact mask 40 over a portion of the conductive contact material 30 that is above source and drain regions of a first fin 42 of the two longer fins 21. The invention follows this by selectively etching regions of the conductive contact material 30 and the semiconductor material 11 that are not protected by the contact mask. Such an etch will not affect the gate 20 or spacers 31. This leaves the conductive contact material 30 only on the source

and drain regions of the first fin 42 and removes source and drain regions of a second fin 41 of the two longer fins 21. Therefore, the contact mask 40 performs two functions by patterning the source and drain contacts and by trimming the unwanted portion of the semiconductor material 11. By utilizing the contact mask 44 in this manner, the invention avoids the need for a separate trim mask.

[0035] Figure 4B is a cross-sectional view along line A-A' in Figure 4A, Figure 4C is a cross-sectional view along line B-B' in Figure 4A, and Figure 4D is a cross-sectional view along line C-C' in Figure 4A. In addition, Figure 5A is a schematic perspective view illustrating the inventive fins 41, 42 intersecting the gate 20, and Figures 5B is a schematic top-view diagram of the structure shown in Figure 5A. These additional views illustrate that the inventive structure produced is a unique FinFET that has a first fin 42 with a central channel region 55 and source and drain regions 56 adjacent the channel region 55. The gate 20 intersects the first fin 42 and covers the channel region 55. The second fin 41 only has a channel region. The second fin 41 is parallel to the first fin 42 and is covered by the gate structure.

[0036] In this unique structure, the second fin 41 has a length equal to the width of the gate structure and the first fin 42 is longer than the second fin 41. The source and drain regions 56 of the first fin 42 extend beyond the gate structure; however, the second fin 41 does not extend beyond the gate structure because that portion of the second fin 41 was trimmed when the source and drain contacts 30 were patterned. The

source and drain contacts 30 only cover the source and drain regions 56 of the first fin 42 and no contacts are positioned adjacent the second fin 41.

[0037] Figure 6A is a schematic top-view diagram illustrating the spacing that is required when a trim mask 53 is utilized and Figure 6B is a schematic top-view diagram illustrating the spacing that can be achieved with the invention when the use of a trim mask is avoided. As shown in Figures 6A, at least one unit of spacing "Z" is created to accommodate for the trim mask 53. In this example half a unit (Z/2) is provided between the trim mask 53 and the adjacent silicon island mask RX (51) and the trim mask itself extends over half a unit (Z/2) beyond the edge of the silicon island mask RX (50) with which the trim mask 53 is associated. To the contrary, as shown in Figure 6B, since no trim mask is used with the invention, the adjacent silicon island mask 51 can be placed within a half unit (Z/2) of the edge of the semiconductor loop 11 (or one unit of spacing(Z) from the adjacent silicon island mask 50). Since the RX size is decreased, a lower parasitic capacitance from the contact region is obtained. A denser layout with simpler layout rules and decreased process cost results.

[0038] Figure 7 is a flow diagram illustrating a preferred method of the invention. More specifically, the method patterns a rectangular sacrificial mandrel 700 on a semiconductor layer, forms mask sidewalls 702 along the vertical surfaces of the mandrel, removes the mandrel 704, and etches portions of the hard-mask not protected by the

sidewalls. After removal of the mask sidewalls, the invention etches portions of the semiconductor layer not protected by the hard-mask 706 to leave a freestanding rectangular loop of semiconductor material having two longer fins and two shorter sections. The invention patterns a rectangular gate conductor 708 over central sections of the two longer fins. The invention dopes portions 710 of the semiconductor material, not covered by the gate conductor, to form source and drain regions in portions of the fins that extend beyond the gate. Next the invention forms insulating sidewalls 712 along the gate conductor and covers the gate conductor and the semiconductor material with a conductive contact material. The conductive material is planarized or etched back until the gate conductor is exposed. Then, the invention forms a contact mask 714 over a portion of the conductive contact material that is above source and drain regions of a first fin of the two longer fins and selectively etches 716 regions of the conductive contact material and the semiconductor material not protected by the contact mask. The selective etching process 716 leaves the conductive contact material on the source and drain regions of the first fin and removes the source and drain regions of a second fin of the two longer fins.

[0039]

Therefore, as shown above, only one mask is added to a conventional CMOS design, namely the "FN" level mask, which is used to define a mandrel 10 about which spacers are formed. The conventional silicon-island mask (RX) is used after the gate lithography and processing (PC) to both define source/drain regions outside the gate and to trim

fins that are not desired for the circuit. This eliminates a "trim" mask (TR) and associated processing. This also eliminates some density loss due to the second-order alignment of RX to TR (both levels normally align to FN) and hence yields a denser design.

[0040] Since the RX size is decreased, a lower parasitic capacitance from the contact region is obtained. A denser layout follows with the small RX size, which in turn results in circuits that reside closer to one another. This translates to shorter interconnections and thus lower wire resistance and capacitance. The end result is lower cost, lower power and faster circuits.

[0041] While the invention has been described in terms of preferred embodiments, those skilled in the art will recognize that the invention can be practiced with modification within the spirit and scope of the appended claims.